REMARKS

This Amendment is being filed in response to the Final Office Action mailed February 12, 2009, which has been reviewed and carefully considered. By means of the present amendment, claims 16 and 20 have been canceled without prejudice and its features included in independent claims 1 and 11, respectively. Accordingly, no new issues requiring a new search have been introduced and entry of the present Amendment is respectfully requested.

Claims 1-14 and 17-19 are pending in the application, claims 15-16 and 20 had been currently canceled without prejudice. Claim 1 and 11 are independent.

In the Final Office Action, claims 11-17 and 20 are rejected under 35 U.S.C. §112, second paragraph. This rejection is respectfully traversed. However, to advance prosecution, claim 11 has been amended for better clarity. It is respectfully submitted that this rejection of claims 11-17 and 20 has been overcome. Accordingly, withdrawal of this rejection is respectfully requested.

In the Final Office Action, claims 1-5, 7-9 and 11-20 under 35 U.S.C. §103(a) over U.S. Patent No. 7,024,538 (Schlansker) in view of U.S. 6,076,159 (Fleck) and U.S. Patent Application Publication No. 2003/0145116 (Moroney). Further, claim 6 is rejected under 35 U.S.C. §103(a) over Schlansker in view of Fleck, Moroney and Official Notice. Claim 10 is rejected under 35 U.S.C. §103(a) over Schlansker in view of Fleck and U.S. 5,208,781 (Matsushima). It is respectfully submitted that claims 1-14 and 17-19 are patentable over Schlansker, Fleck, Moroney, Official Notice, and Matsushima for at least the following reasons.

In the Final Office Action, it is correctly noted on page 5 that Schlansker does not disclose or suggest an instruction address modification circuit that includes an offset register connected to an output of a functional unit that updates an offset value in the offset register during the execution of a program. Moroney is cited in an attempt to remedy the deficiencies in Schlansker.

Moroney is directed to a system that enables communication between two networks having different network protocols. As shown in FIG 8 and specifically recited in Paragraph [0095] of Moroney, an "instruction controller 54 ... accepts input from the translate

block 74. An example of such input is the offset stored in the translation memory 80 as shown in FIG. 7." That is, the translate block 74 is connected to the input of the controller 54 to provide the offset to the controller 54.

It is respectfully submitted that Schlansker, Moroney, and combinations thereof, do not disclose or suggest the present invention as recited in independent claim 1, and similarly recited in independent claim 11 which, amongst other patentable elements, recites (illustrative emphasis provided):

> wherein the instruction address modification circuit includes an offset register connected to an **output** of a functional unit of the plurality of functional units, the functional unit updating an offset value in the offset register during the execution of the program.

These features are nowhere taught or suggested in Schlansker and Moroney, alone or in combination. Rather, Moroney discloses a translate block 74 which is connected to the **input** of the controller 54 to provide an offset to the controller 54.

In addition, it is respectfully submitted that Schlansker, Moroney, and combinations thereof, do not disclose or suggest the present invention as recited in independent claim 1, and similarly

recited in independent claim 11 which, amongst other patentable elements, recites (illustrative emphasis provided):

> wherein the instruction address modification circuit is operationally coupled to a **controller** that provides the instruction address, **and** to one of the plurality of the functional units that provides an adjust signal to the instruction address modification circuit; the instruction address modification circuit being configured to modify the translation in response to the adjust output and to provide a modified translated address to one of the plurality of the memory units.

Having an instruction address modification circuit, a memory, and both a controller and a functional unit, where the controller is distinct from the functional unit, is nowhere disclosed or suggested in Schlansker and Moroney, alone or in combination. This dichotomy of the controller and the functional unit are recited in independent claims 1 and 11. Fleck, Official Notice, and Matsushima are cited to allegedly show other features and do not remedy the deficiencies Schlansker and Moroney. Accordingly, it is respectfully submitted that independent claims 1 and 11 are allowable, and allowance thereof is respectfully requested. In addition, it is respectfully submitted that claims 2-10, 12-14 and 17-19 should also be allowed at least based on their dependence

from independent claims 1 and 11.

Further, the Official Notice regarding the rejection of claim 6 is respectfully traversed. If it is well known to translate two instruction addresses to the same physical address for a particular memory unit is in fact well known, as alleged in rejecting claim 6, then it should be described in documents that the Examiner can provide. Without access to these documents, Applicants cannot evaluate whether it is obvious to one of ordinary skill in the art to combine them with the references already of record. Such documentation is accordingly respectfully requested.

In addition, Applicants deny any statement, position or averment of the Examiner that is not specifically addressed by the foregoing argument and response. Any rejections and/or points of argument not addressed would appear to be moot in view of the presented remarks. However, the Applicants reserve the right to submit further arguments in support of the above stated position, should that become necessary. No arguments are waived and none of the Examiner's statements are conceded. And in particular, no Official Notices are conceded.

In view of the above, it is respectfully submitted that the present application is in condition for allowance, and a Notice of Allowance is earnestly solicited.

Respectfully submitted,

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